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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,171	02/03/2006	Martin J. Edwards	GB030133US1	9639

24738 7590 11/03/2008

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
MORRIS, JOHN J	

ART UNIT	PAPER NUMBER
4147	

MAIL DATE	DELIVERY MODE
11/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,171	EDWARDS ET AL.	
	Examiner	Art Unit	
	JOHN J. MORRIS	4147	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/10/2006, 02/03/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 19-21, and 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomooka et al. (US Pat# 5909262/ *or "Tomooka" hereinafter*).

For **claim 1,** Tomooka teaches an amplification circuit (Tomooka, column 2, lines 36-38) comprising: an input to which an input voltage is provided (Tomooka, figure 5, item 4), a capacitor arrangement (Tomooka, figure 5, items 6 and 7), and a switching arrangement (Tomooka, figure 5), wherein the capacitor arrangement comprises a first capacitor which has a voltage dependent capacitance (Tomooka, figure 5, item 7) and a second capacitor (Tomooka, figure 5, item 1) wherein the circuit is operable in two modes, a first mode in which the input voltage is provided to one terminal of at least the first capacitor (Tomooka, column 4, lines 24-39) and a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors such that the voltage across the first capacitor changes to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3), the output voltage being dependent on the resulting voltage across the first capacitor (Tomooka, column 5, lines 3-35).

For **claim 2,** Tomooka teaches a switching arrangement comprising an input switch for selectively coupling the input voltages to the capacitor arrangement, wherein the first mode the input switch couples the input voltage to the capacitor arrangement, and in the second mode the input switch isolates the input voltage to the capacitor arrangement (Tomooka, column 4, lines 39-50).

For **claim 3,** Tomooka teaches a voltage on one terminal of the first and/or second capacitor is changed (Tomooka, column 4, line 44).

For **claim 4,** Tomooka teaches wherein the change in voltage on the one terminal of the capacitor results in a reduction in capacitance (Tomooka, column 4, line 46).

For **claim 19,** Tomooka teaches a circuit wherein the voltage dependent capacitor comprises a transistor with source and drain connected together, and wherein the one terminal is defined by the gate and the other terminal is defined by the connected source and drain (Tomooka, column 5, lines 49-55 and figure 11).

For **claim 20,** Tomooka teaches a circuit wherein the voltage dependent capacitor comprises a transistor with source and drain connected together, and wherein the one terminal is defined by the gate and the other terminal is defined by the connected source and drain (Tomooka, column 5, lines 49-55 and figure 11). Tomooka does not

specifically state that the transistor may be a thin film MOS transistor; however, it would have been obvious to one of ordinary skill in the art that the transistor may be a MOS transistor because there are MOS FET as well as n-type and p-type MOS transistors. It also would have been an obvious matter of design choice as to what type of transistor to use since it would only require a mere change of component of the circuit.

For **claim 21**, Tomooka teaches an active matrix device comprising an array of device elements and circuitry for generating control signals for controlling the device elements, further comprising a circuit for increasing the voltage level of the control signals before supply to the device elements (Tomooka, abstract). Tomooka teaches an LCD with driving circuitry, which is well known to be an active matrix device which comprises an array of device elements.

For **claim 23**, Tomooka teaches an active matrix device comprising an array of pixels and circuitry for generating control signals for controlling the device elements, further comprising a circuit for increasing the voltage level of the control signals before supply to the device elements (Tomooka, abstract). Tomooka teaches an LCD with driving circuitry, which is well known to be an active matrix device which comprises an array of pixels.

For **claim 24,** Tomooka teaches storing a display pixel voltage on a storage capacitor, providing a voltage to the display pixel in dependence on the stored display pixel voltage, wherein the writing circuitry comprises the control transistor, the gate voltage of the control transistor being provided by the storage capacitor arrangement, and wherein the storage capacitor arrangement comprises the capacitor arrangement of the amplification circuit (Tomooka, column 4 line 40 - column 5 line 35, figure 5).

Claim 25 is rejected upon the same grounds as claim 21.

For **claim 26**, Tomooka teaches an active matrix device comprising an array of pixels and circuitry for generating control signals for controlling the device elements, further comprising a circuit for increasing the voltage level of the control signals before supply to the device elements (Tomooka, abstract). Tomooka teaches an LCD with driving circuitry, which is well known to be an active matrix device which comprises an array of pixels.

Claim 27 is rejected upon the same grounds as claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomooka et al. (US Pat# 5909262/ *or "Tomooka" hereinafter*) in view of Miyake et al. (US Pat# 6788108 B2/ *or "Miyake" hereinafter*)

For **claim 5,** Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Miyake teaches a circuit which uses two voltage dependent capacitors (Miyake, figure 21, items 2154 and 2155). These capacitors are made using transistors, therefore they are voltage dependent. The applicant also teaches that the second capacitor may also be voltage-dependent; this shows that it is also a matter of design choice. It would have been obvious to one of ordinary skill in the art to modify Tomooka with Miyake because both are semiconductor devices that can be used with LCD's and using two voltage dependent capacitors would give the designer greater control on the voltage applied to the pixel which would affect the image quality.

For **claim 6,** Tomooka teaches that the voltage across the first capacitor changes to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3). Therefore it would have been obvious that a change in voltage on the one terminal of the second capacitor would also result in a reduction in capacitance.

For **claim 7,** Tomooka teaches that the voltage across the first capacitor can change to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3). It would have been an obvious matter of design choice to change the voltage across the second capacitor while changing the voltage across the first capacitor since such a modification would only require changing the control voltage applied to the second capacitor. Miyake teaches a separate input for each capacitor, therefore this would allow one of ordinary skill in the art to apply two different voltages to the capacitors (Miyake, figure 21).

Claim 8 is rejected upon the same grounds as claim 7.

For **claim 9,** it is well known in the art that a transistor is an example of a switch that can be controlled by voltage. Therefore, one could use a voltage dependent capacitor which comprises transistors for the input switch. Also, Miyake teaches an input to the gate of a capacitor (Miyake, figure 21, item 2155). It would have been obvious to one of ordinary skill in the art to modify Tomooka with Miyake because both are semiconductor

devices that can be used with LCD's and the addition of Miyake would allow a high load driving capability as well as a short rise time.

Claim 10 is rejected upon the same grounds as claim 9.

For **claim 11,** Tomooka teaches that the voltage across the first capacitor can change to reduce the capacitance of the first capacitor (Tomooka, column 4 line 40 - column 5 line 3). Tomooka does not teach using two voltage dependent capacitors; however, in the same field of endeavor, Miyake teaches a circuit which uses two voltage dependent capacitors (Miyake, figure 21, items 2154 and 2155). These capacitors are made using transistors, therefore they are voltage dependent. The applicant also teaches that the second capacitor may also be voltage-dependent; this shows that it is also a matter of design choice. Miyake teaches two transistors in parallel with each other with the gate of the second transistor connected to the one terminal of the second capacitor (Miyake, figure 21, item 2155 or 2154).

For **claim 12,** Tomooka does not teach a switching arrangement with multiple switches; however in the same field of endeavor, Miyake teaches using multiple switches (Miyake, figure 21). Miyake teaches switches coupling reference, control, and input voltage to the terminals of the first and second capacitor (Miyake, figure 21 and figure 6c). It would have been obvious to one of ordinary skill in the art to modify Tomooka with Miyake because both are semiconductor devices that can be used with LCD's and

the addition of Miyake would allow a high load driving capability as well as a short rise time.

For **claim 13,** Miyake teaches the first switch and input switch closed so that a voltage across the capacitors is dependent on the input voltage (Miyake, figure 21 and 6c) and where the second switches are closed and the output voltage comprises the voltage on the other terminals of the first and second capacitors(Miyake, figure 21 and 6c).

For **claim 14,** Miyake teaches capacitors comprising thin film transistors (Miyake, column 25, lines 3-12). It is obvious that thin film transistors may be n-type MOS devices.

Claim 15 is rejected upon the same grounds as claim 14.

For **claim 16,** Miyake teaches an input connected to on terminal of the first and second capacitors and respective control voltages are coupled to the other terminals of the first and second capacitors through respective control switches (Miyake, figure 6c, items 653 and 654). It would have been obvious to one of ordinary skill in the art to modify Tomooka with Miyake because both are semiconductor devices that can be used with LCD's and the addition of Miyake would allow a high load driving capability as well as a short rise time.

For **claim 17,** Tomooka and Miyake do not teach a shorting switch; however it would have been obvious if one desired a shorting switch to add one between the terminals of the first and second capacitors, since such a modification only requires adding one switch whose functionality is adequately described in its name "shorting switch".

For **claim 18,** these limitations are already described and rejected in claim 13, except for the addition of the shorting switch. However, Miyake teaches where the connection between those two terminals of the capacitors is a short, which would be the same thing as if a shorting switch was there and closed.

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tomooka et al. (US Pat# 5909262/ *or "Tomooka" hereinafter*) in view of Abe. (US Pat# 5694369).

For **claim 22**, Tomooka does not teach a latch circuit; however, in the same field of endeavor, Abe teaches an amplification circuit with an output data latch circuit (Abe, figure 1, items 6 and 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tomooka with Abe because both are semiconductor devices with amplification circuits and the addition of an output data latch circuit can improve stability.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sano (US Pub# 20050018503 A1) discloses an amplifier circuit; Sano et al. (US Pub# 20050017929 A1) disclose a pixel circuit and display device; Marr (US Pat# 4021788) discloses a capacitor memory cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN J. MORRIS whose telephone number is (571)270-7171. The examiner can normally be reached on Monday - Friday 7am - 3pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kieu-Oanh Bui can be reached on (571)272-7291. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KIEU-OANH BUI/
Supervisory Patent Examiner, Art Unit 4147

JOHN J MORRIS
Examiner
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